SBN & DUNE Coordination

MAY 8TH, 2015

Outline

- LAr TPC Projects
- Key Developments with Commonalities
- System Integration
- Summary

LAr TPC Projects

- Short Base Program
  - MicroBooNE
  - SBND
  - ICARUS
- DUNE
  - 35 ton
  - DUNE-Test@CERN
  - 10 kt & 40 kt

Key Developments with Commonalities

- Key Developments
  - TPC electrode system (resistive cathode, field cage, sense wire planes)
  - Cold electronics
    - FE ASIC
    - ADC ASIC
    - Cold FPGA and/or integrated ASIC
    - Cold mother board, connections to sense wires
  - Cold cables
  - Signal feed-through
- ***A program should be established to build a full cold readout system, from TPC electrode to the signal feed-through, for system tests of APA (at each step, following fabrication, transport and installation in the cryostat).***

System Integration

- Each key component will have a dedicated test stand and QA plan
  - This includes ASICs, boards, cables, feed-throughs, etc.
  - This has been done before for both ATLAS (~10,000 boards, ~150 feed-throughs & cables) and MicroBooNE (~2,000 ASICs, ~500 boards, ~13 feed-throughs & cables)
- ***Emphasis should be put on the system integration***
  - System integration is crucial to understand detector performance and finalize the design
  - Various integration tests have been done for both ATLAS (at BNL & CERN) and MicroBooNE (at BNL & Fermilab)
  - System integration, in both SBN experiments and DUNE-Test at CERN, will serve as crucial steps towards a successful construction of DUNE

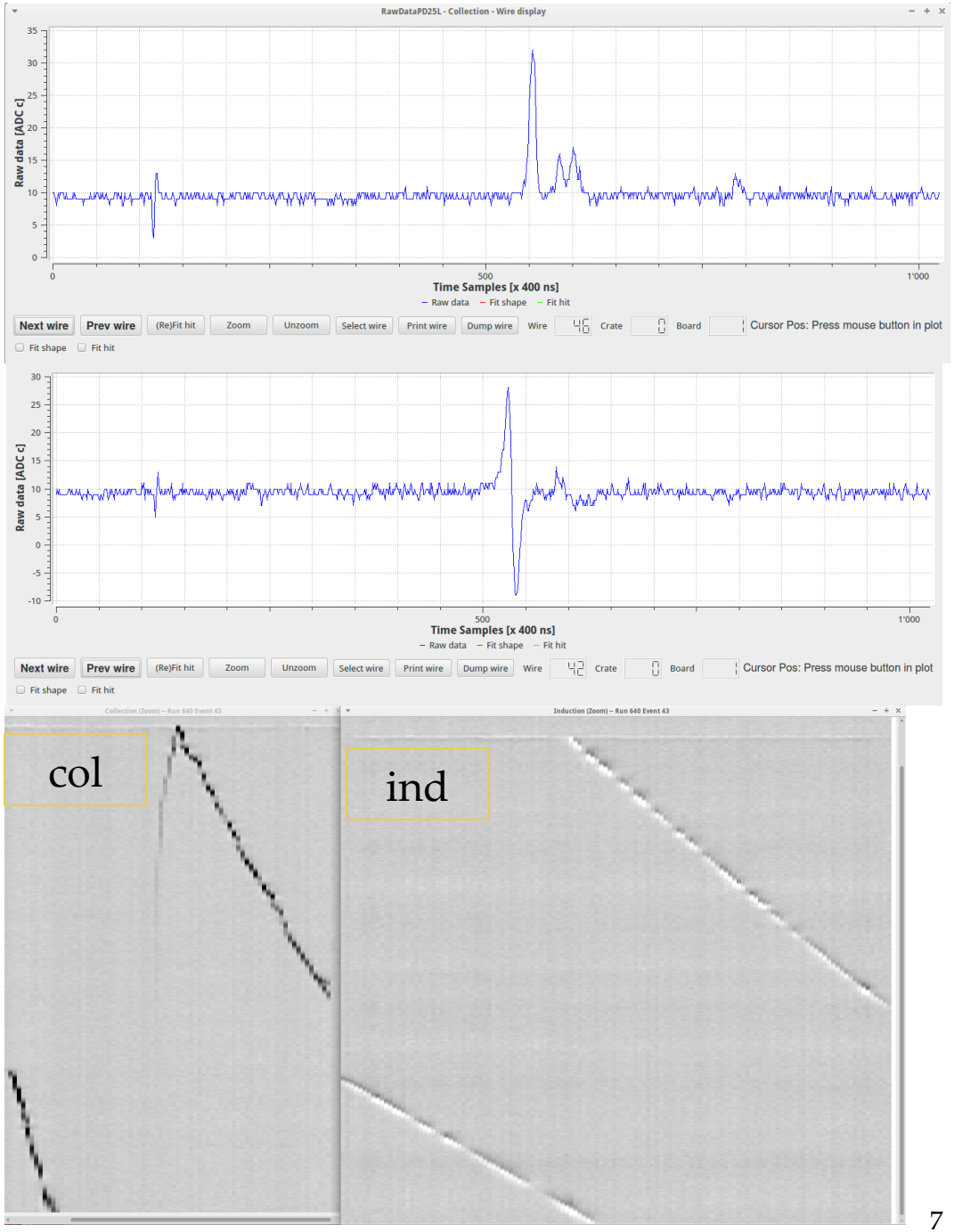
Cold Electronics & System Integration

	Cold Electronics	System Integration	Year of Construction
MicroBooNE	FE ASIC	*Feedback to ICARUS*	*2013*
35 ton	FE ASIC	*Feedback to SBND*	*2014-2015*
	ADC ASIC		
	Cold FPGA		
ICARUS	Optimized FE ASIC	*Feedback to SBND*	*2015*
SBND	FE ASIC w. Pulser	*Feedback to DUNE-Test@CERN*	*2017*
	Optimized ADC ASIC		
	Cold FPGA		
DUNE-Test@CERN	FE + ADC + FPGA		*2018*
	Integrated ASIC	*Feedback to DUNE*	
DUNE - 10 kt	Integrated ASIC		*2020*

BLUE	SBN
RED	DUNE
GREEN	New Development

System Integration Example:

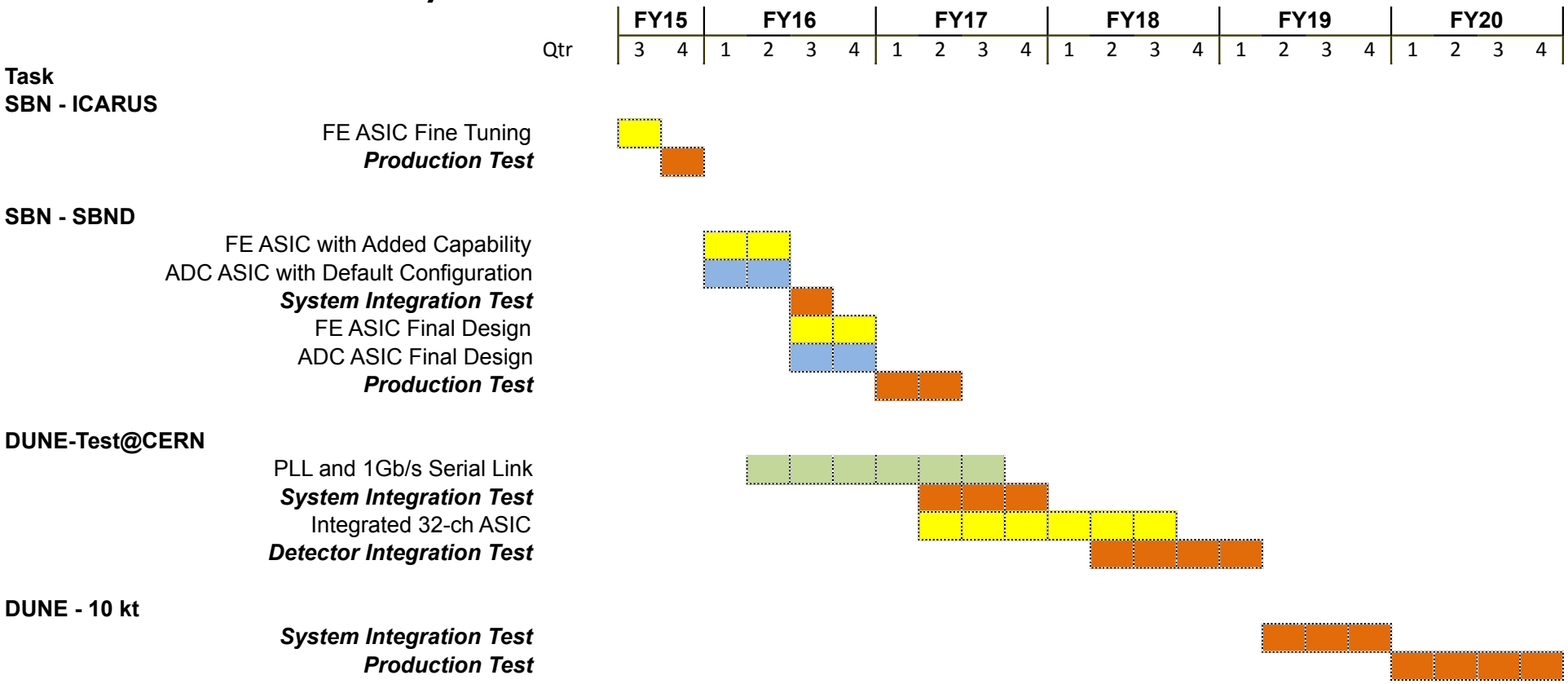
- ICARUS 50l TPC
  - Warm integration test in the week of March 30th at CERN
  - Cold data taking in the week of April 20th at CERN:
    - **The signals were observed and the tracks reconstructed on the first day of cooling down!**



Importance of System Integration

- CAPTAIN
  - Complete design of MicroBooNE readout electronics was given to LANL
  - All ASICs were tested at BNL
  - All cold mother boards were tested at BNL in September 2013
  - **No good data or track after 18 months !? It is instructive to analyze why?**

Preliminary Plan



- Only development of ASIC components are listed
  - Boards, cable & FT are not listed for clear presentation of the plan
- A continuous integration and production test program in next 4-5 years, across SBN and DUNE, to ensure a successful construction of DUNE

Summary

- Key developments for LAr TPC projects share many commonalities in basic technical aspects
- We plan to build a full cold readout system, from TPC electrode to the signal feed-through, for system test of APA
  - QA procedure of individual components will be established along this development
  - Resources should be shared and optimized between SBN and DUNE
- System integration, in both SBN experiments and DUNE test at CERN, will serve as crucial steps toward a successful construction of DUNE
  - All experiments should benefit from both scientific and technical developments from each one of them

Backup Slides

LAr TPC Projects in SBN & DUNE

- MicroBooNE
  - TPC electrode
  - Cold electronics
    - FE ASIC
    - Cold mother board
  - Cold cable
  - Signal feed-through
  - Warm interface electronics
  - Warm Cable
  - Digitization electronics
- 35 ton
  - TPC electrode
  - Cold electronics
    - FE ASIC
    - ADC ASIC
    - Cold FPGA
    - Cold mother board
  - ADC ASIC that was developed is not just a simple multi-channel ADC, but it also provides S/H at the input and buffering, multiplexing and serialization at the output
  - The multiplexing degree and channel number can also be increased, if the application requires

Scale of Small LAr TPC Projects in SBN & DUNE

- MicroBooNE
  - ***8,256 channels***
  - 516 FE ASICs
  - 50 cold mother boards
  - 11 sets of cold cable (269)
  - 11 sets of signal feed-through
  - 269 warm interface boards
  - 11 sets of warm cable (258)
  - 129 receiver & ADC boards
- 35 ton
  - ***2,048 channels***
  - 128 FE ASICs
  - 128 ADC ASICs
  - 16 cold FPGAs
  - 16 cold mother boards

LAr TPC Projects in SBN & DUNE

- SBND
  - TPC electrode
  - Cold electronics
    - FE ASIC
    - ADC ASIC
    - Cold FPGA
    - Cold mother board
  - Cold cable
  - Signal feed-through
  - Warm interface electronics
- ICARUS
  - Cold electronics
    - FE ASIC
    - Cold mother board
- DUNE-Test@CERN
  - TPC electrode
  - Cold electronics
    - FE ASIC/ADC ASIC/Cold FPGA
    - ***Or*** Integrated ASIC
    - Cold mother board
  - Cold cable
  - Signal feed-through
- DUNE
  - TPC electrode
  - Cold electronics
    - FE ASIC/ADC ASIC
    - ***Or*** Integrated ASIC
    - Cold mother board
  - Cold cable
  - Signal feed-through

Scale of LAr TPC Projects in SBN & DUNE

- SBND
  - ***11,264 channels (sense wires)***
  - 704 FE ASICs
  - 704 ADC ASICs
  - 88 cold FPGAs
  - 88 cold mother boards
  - 4 sets of cold cable
  - 4 sets of signal feed-through
  - 32 warm interface boards
- ICARUS
  - ***53,248 channels***
  - 3,328 FE ASICs
  - 832 cold mother boards
- DUNE-Test@CERN
  - ***15,360 channels***
  - 960 FE ASICs/960 ADC ASICs/ 120 cold FPGAs
  - ***Or*** 480 integrated ASICs
  - 120 cold mother boards
  - 3 sets of cold cable
  - 3 sets of signal feed-through
- DUNE 10 kt
  - ***384,000 channels***
  - 24,000 FE ASICs/24,000 ADC ASICs
  - ***Or*** 12,000 integrated ASICs
  - 3,000 cold mother boards
  - 75 sets of cold cable
  - 75 sets of signal feed-through